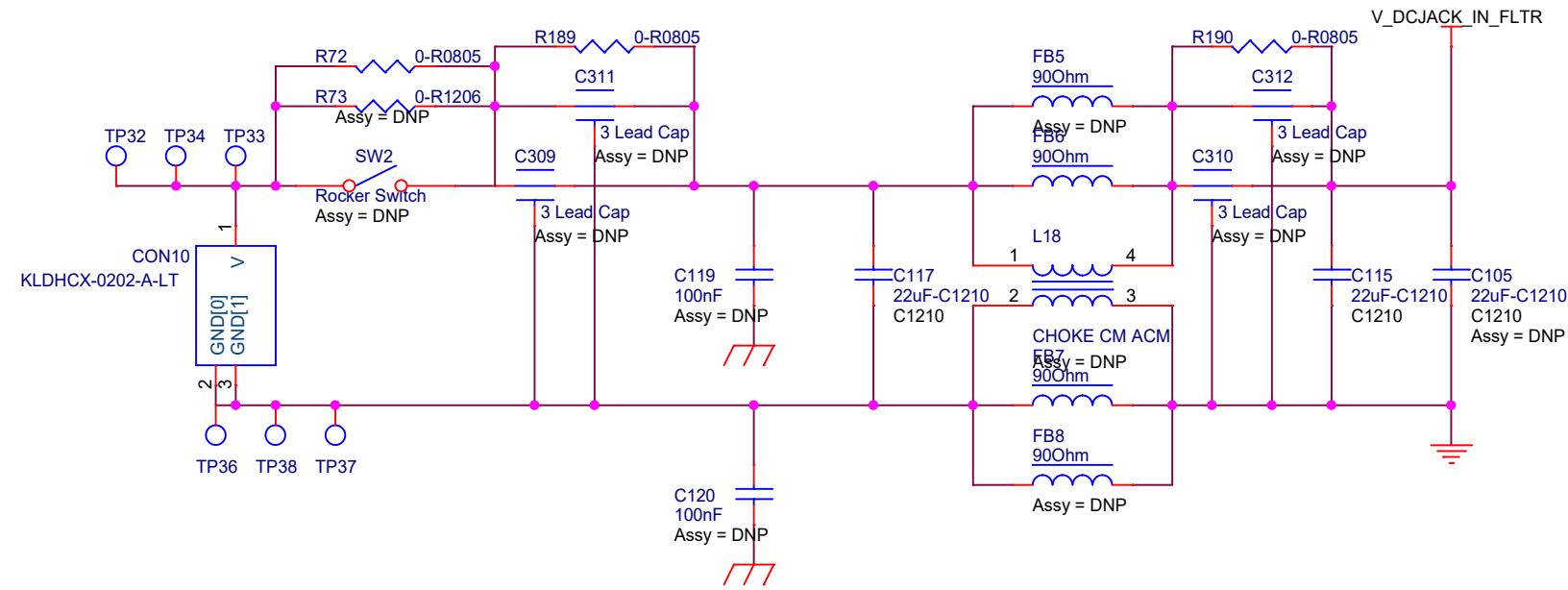
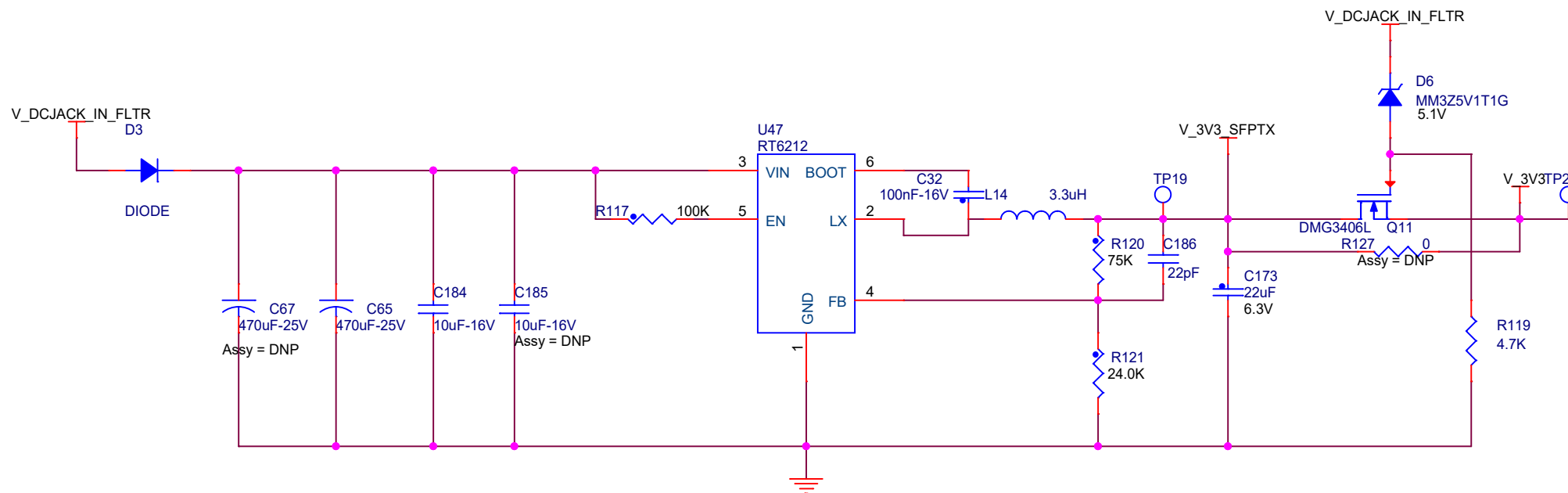
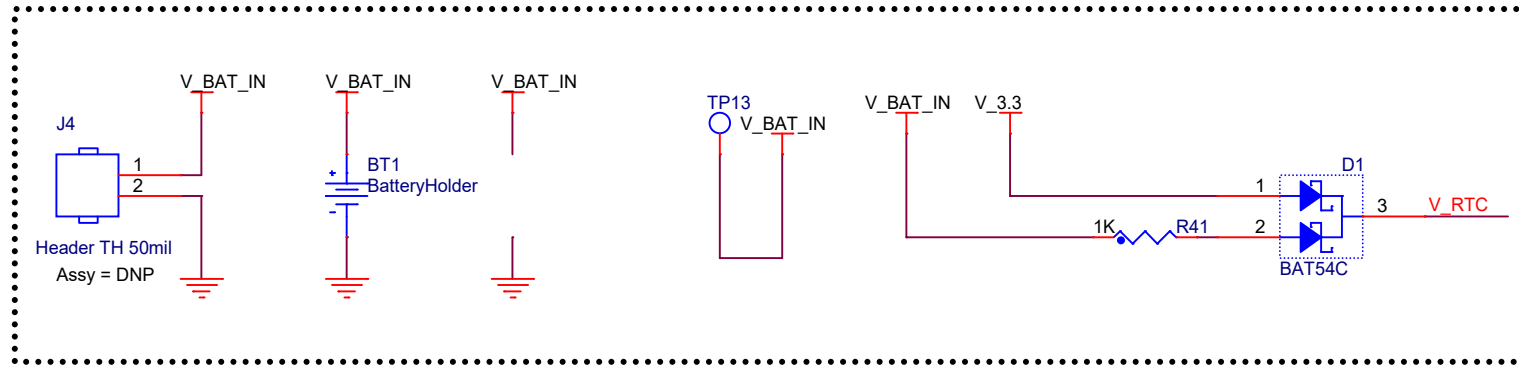



Power Jack

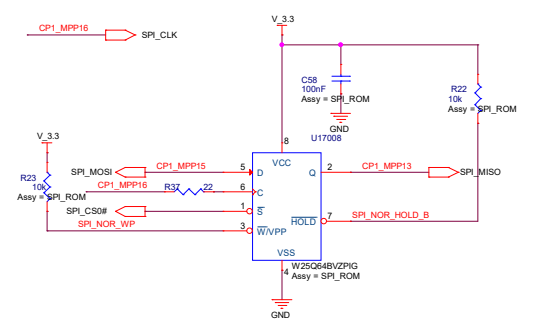


RTC Voltage 3.0v battery

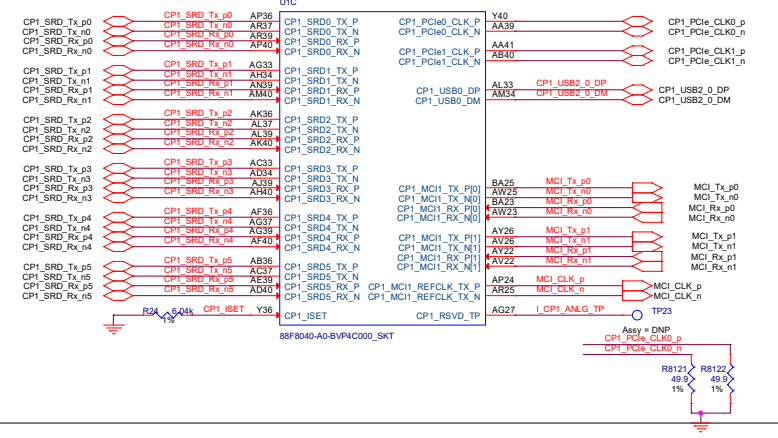


| | | |
|---|------------------------|---|
|  | | Copyright (c) 2014 SolidRun Ltd. Released under Creative Commons Attribution 3.0 Unported License All Rights Reserved |
| Size | Title | Rev |
| B | DC input and RTC | 1.1 |
| Date: | Monday, March 11, 2019 | Sheet 1 of 10 |

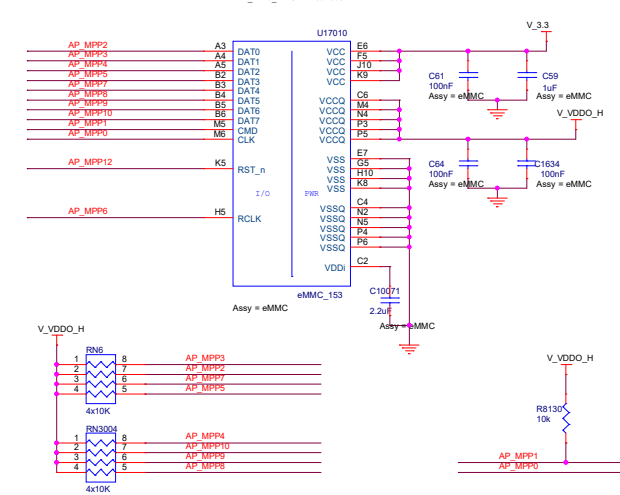
64Mb SPI flash (bootable)



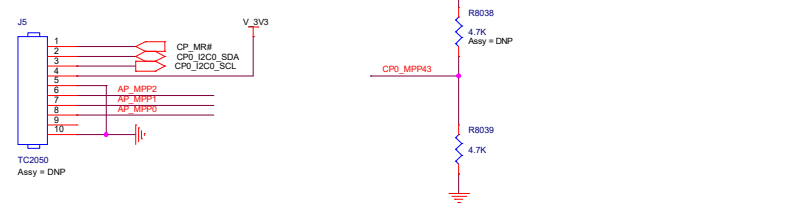
8040 SERDESes



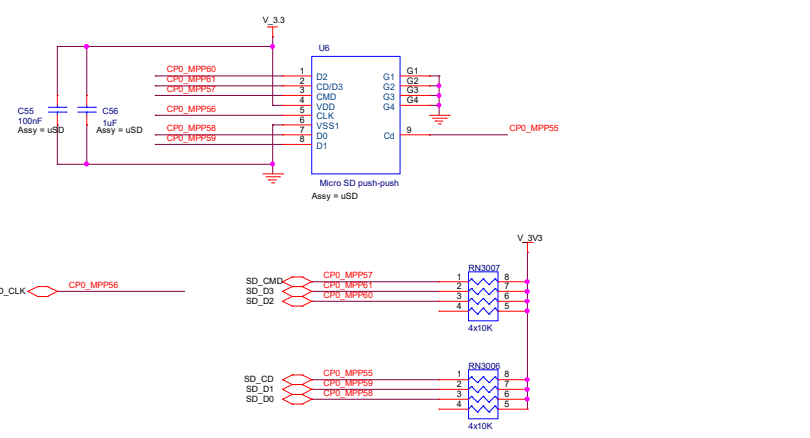
eMMC (bootable)



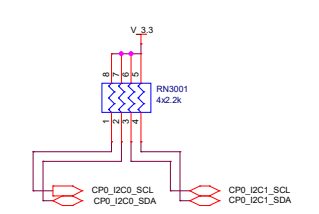
TAG Connect



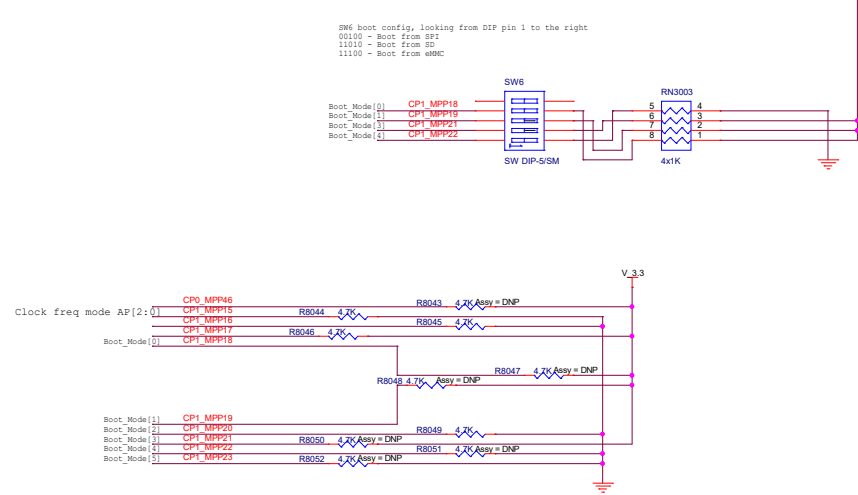
micro SD connector (bootable)



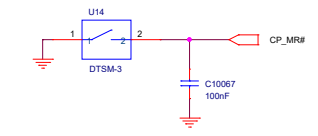
SFP+ I2C pullups



Armada 8040 Boot Select

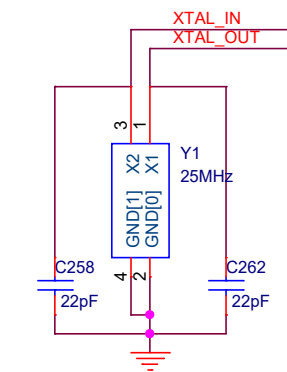
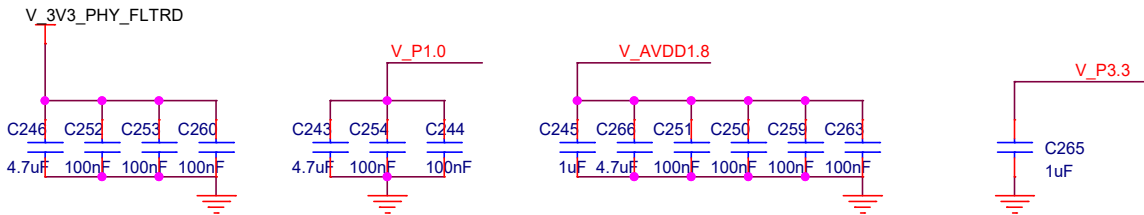
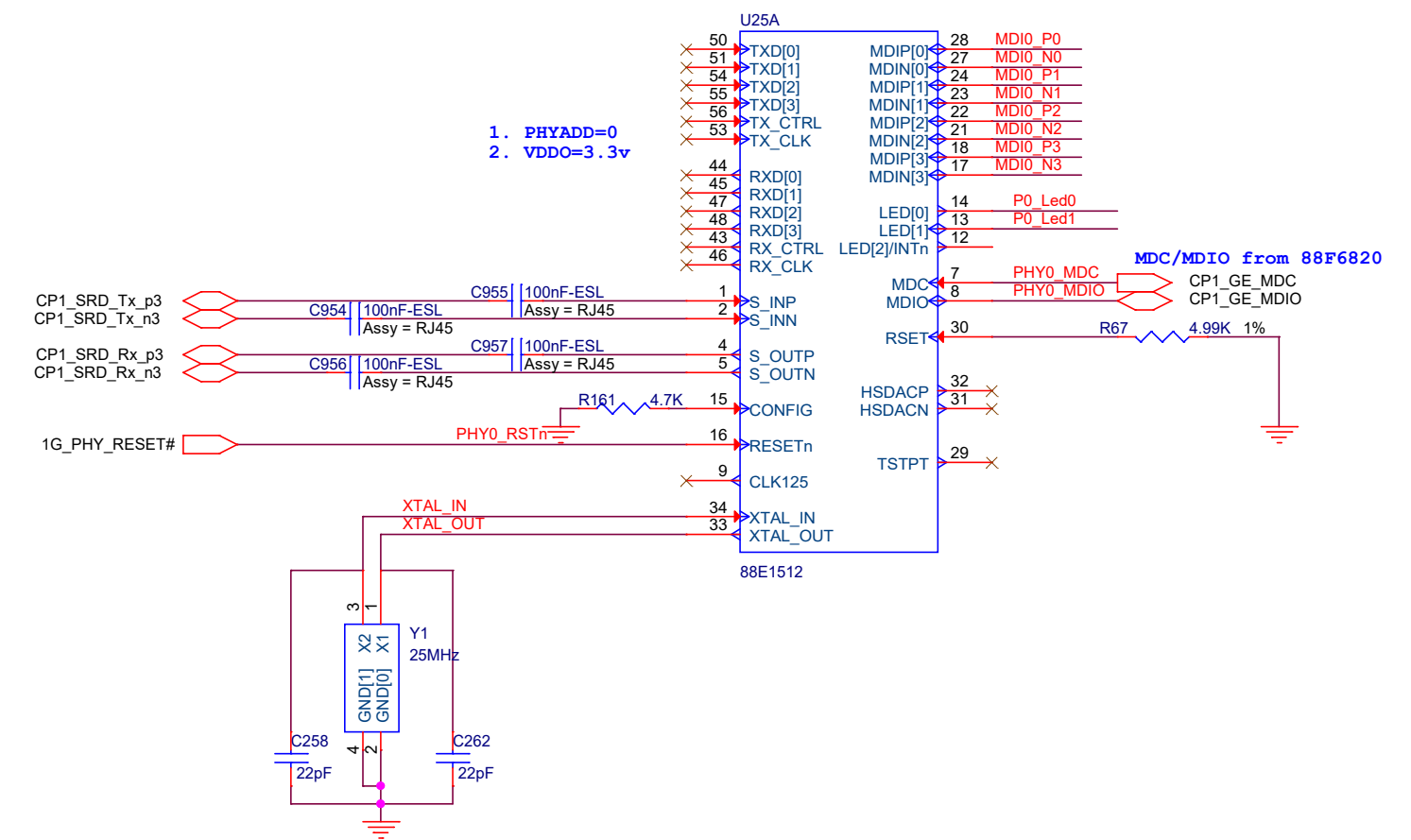
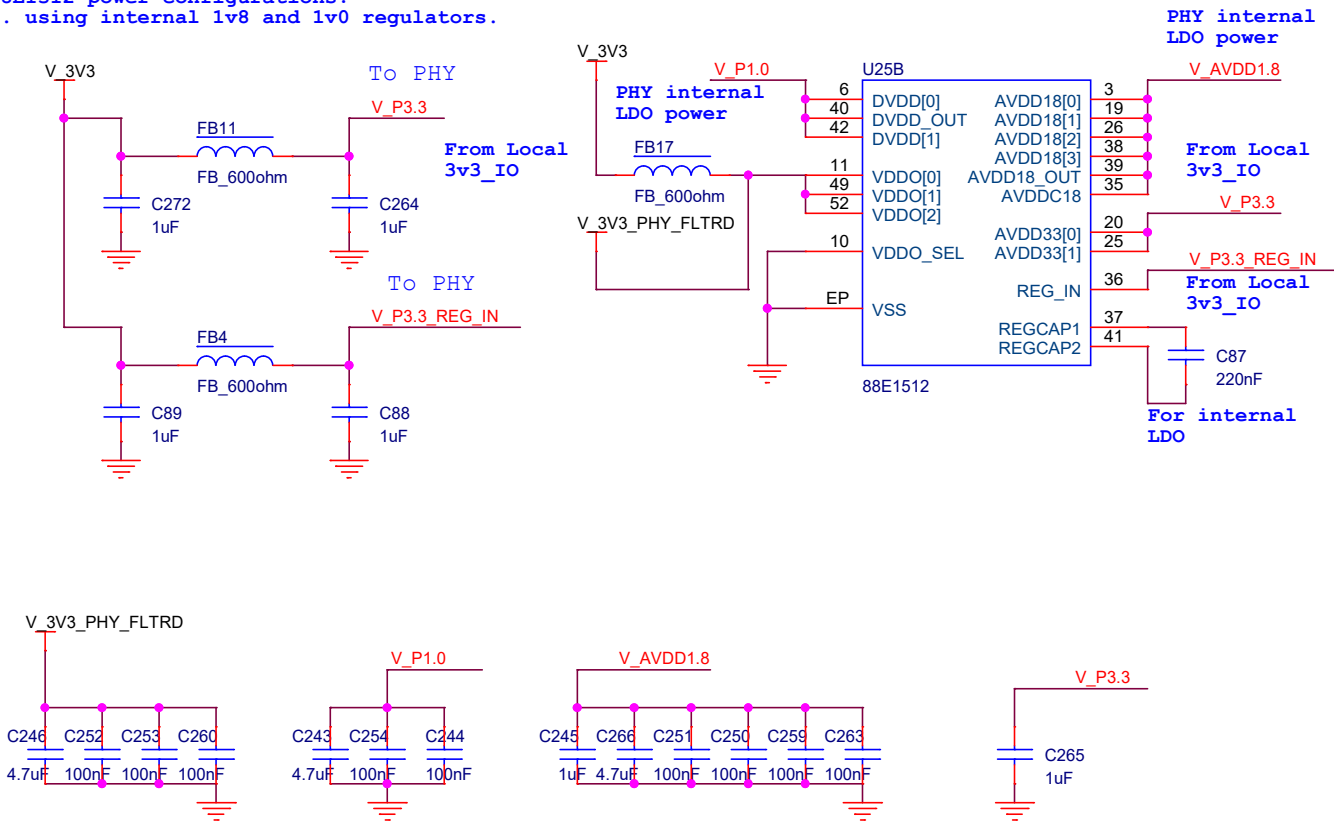


Reset logic



PHY Power configurations

88E1512 power configurations:
1. using internal lv8 and lv0 regulators.



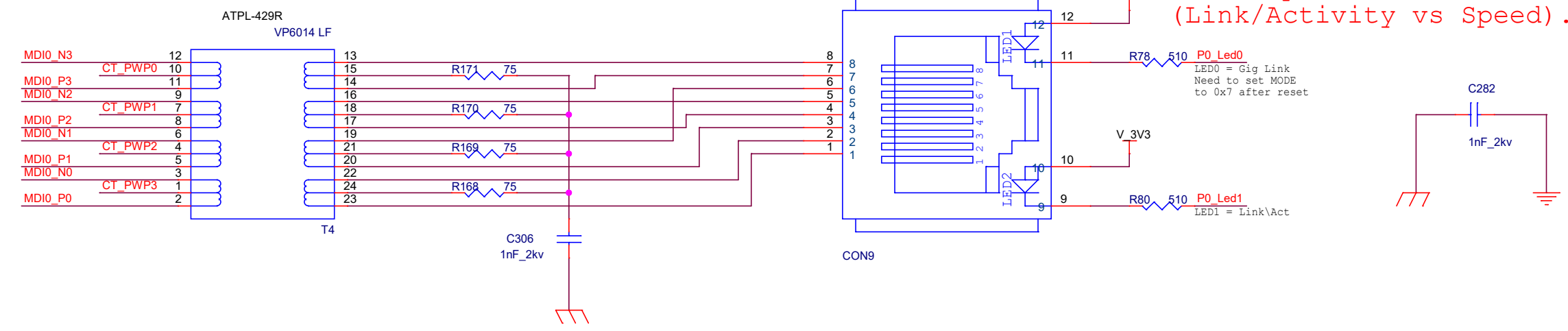
PHY0 - RGMII0 Function as GEO Port PHYADD configuration

88E1512 PHY configuration options:
PHY_address=1

Table 53: Configuration Mapping

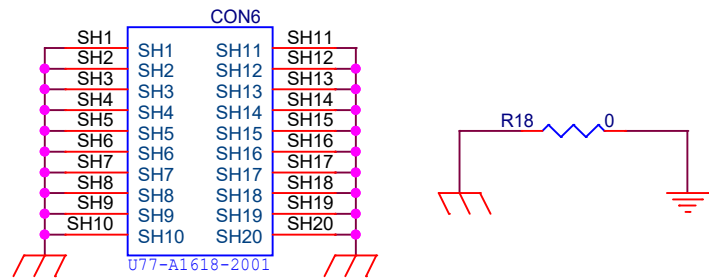
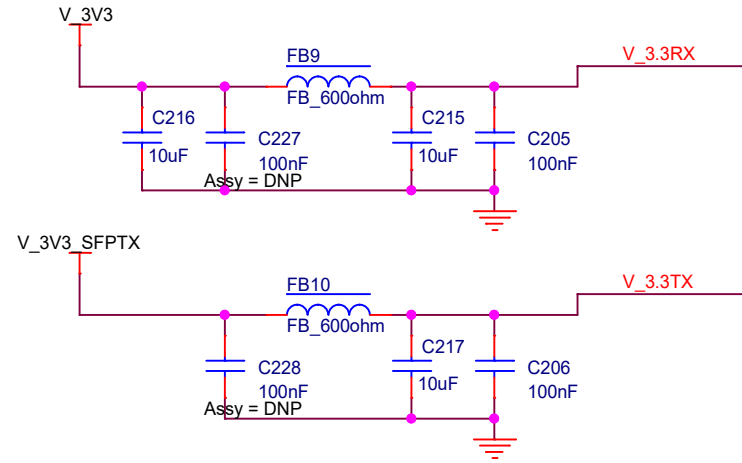
| Pin | CONFIG Bit1 | CONFIG Bit 0 | Value Assignment |
|--------|-------------|--------------|--|
| CONFIG | 0 | 0 | PHYAD[0] = 0 VDDO_LEVEL ¹ = 3.3V |
| CONFIG | 1 | 1 | PHYAD[0] = 1 VDDO_LEVEL ¹ = 3.3V |
| CONFIG | 1 | 0 | PHYAD[0] = 0 VDDO_LEVEL ¹ = 2.5V |
| CONFIG | 0 | 1 | PHYAD[0] = 1 VDDO_LEVEL ¹ = 2.5V |

¹ This is valid only for 88E1510/88E1512. For 88E1513, the VDDO_LEVEL is fixed at 1.8V, hence the bit mapping for VDDO_LEVEL is ignored.

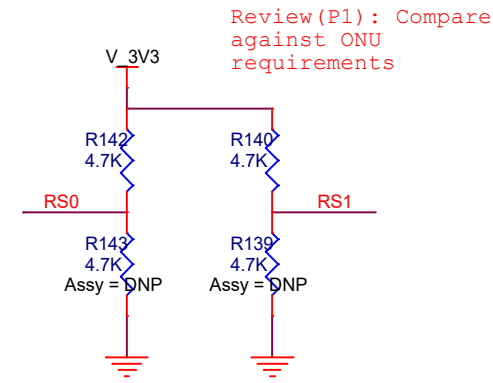
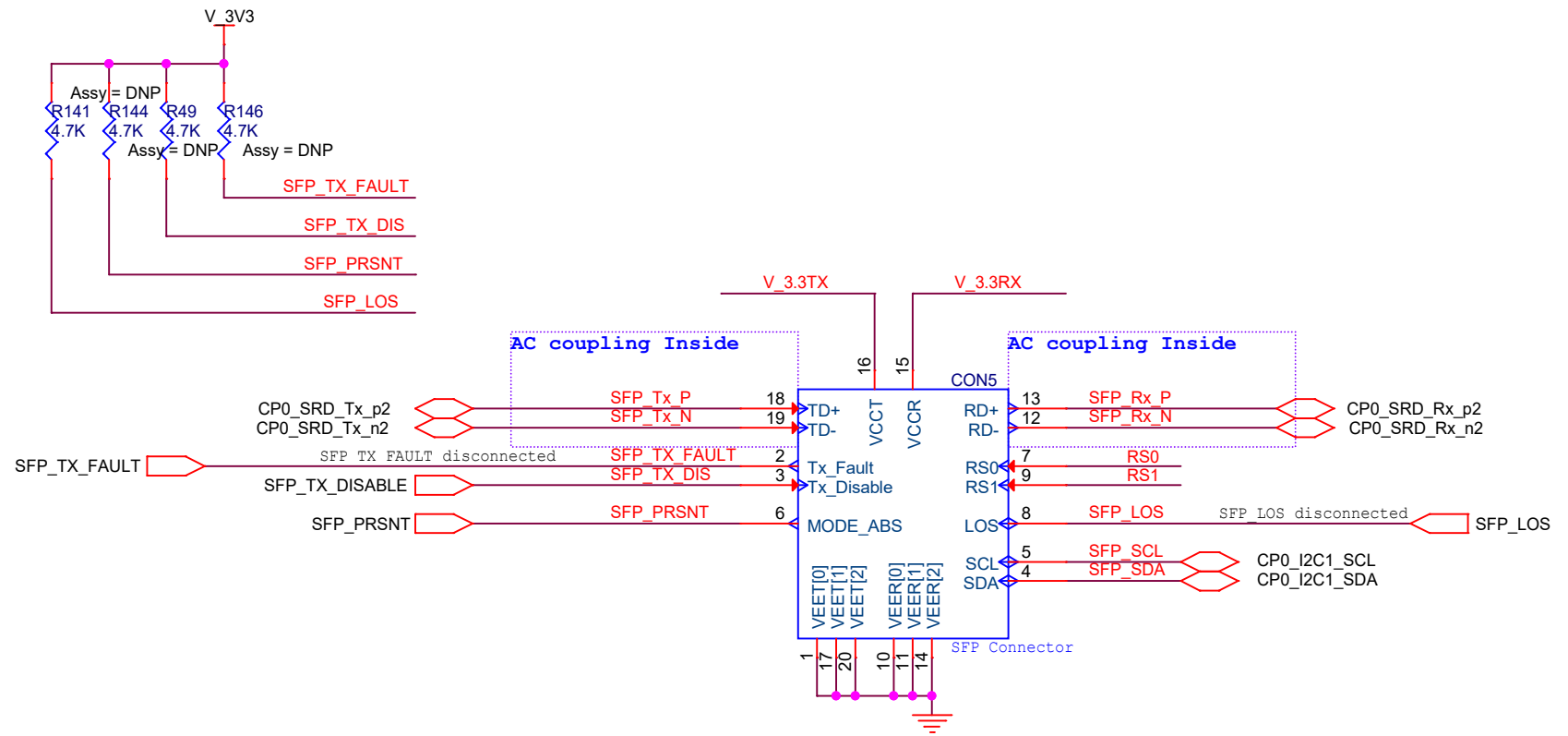


Review(P2): Make sure LED connection according to common practice (Link/Activity vs Speed).

Notice that SFP TX supply is separated from the other.
This supplies ONUs with more than 10msec when suddent
power failure occurs.



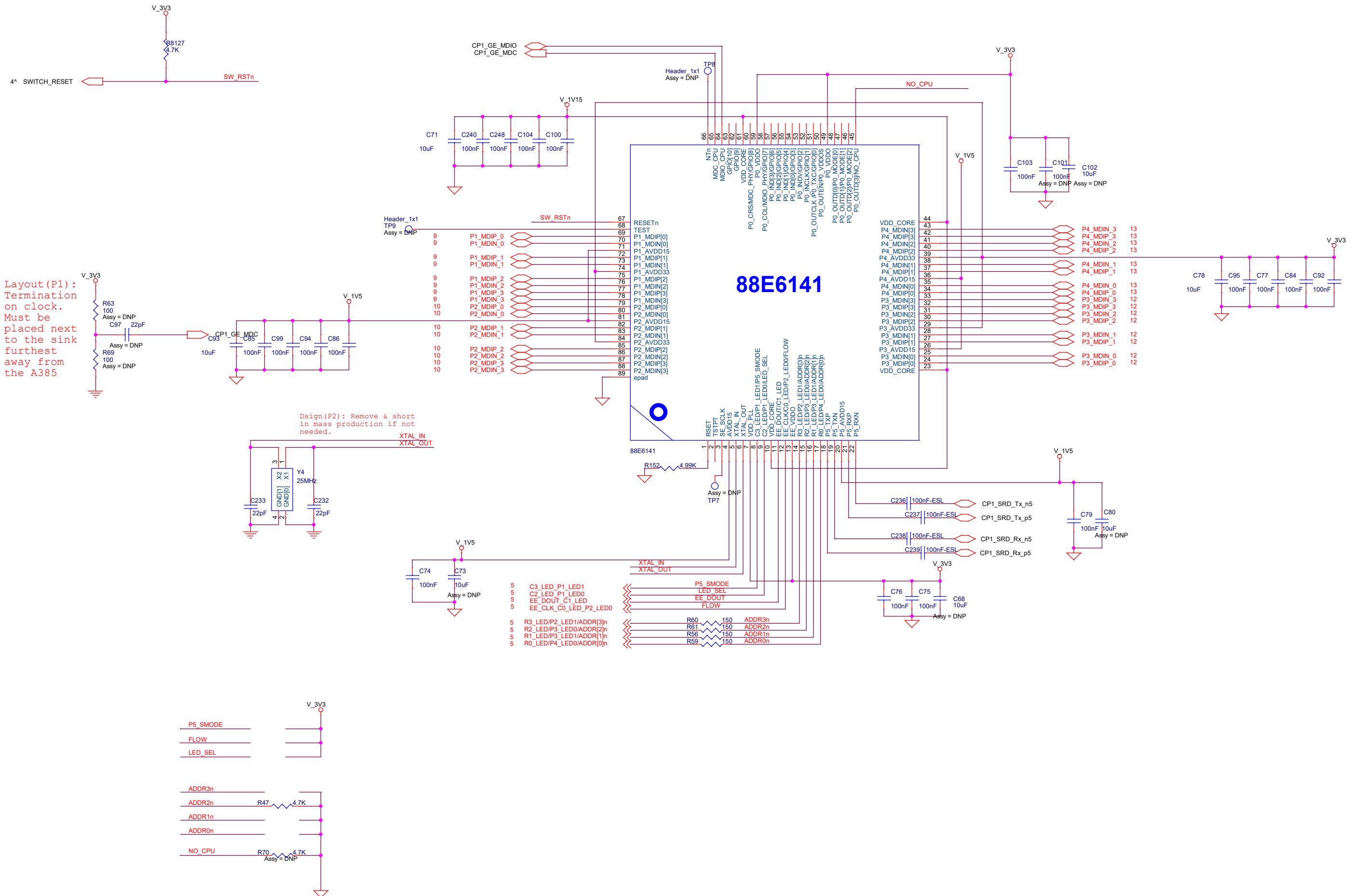
SFP connector



Review (P1) : Compare
against ONU
requirements

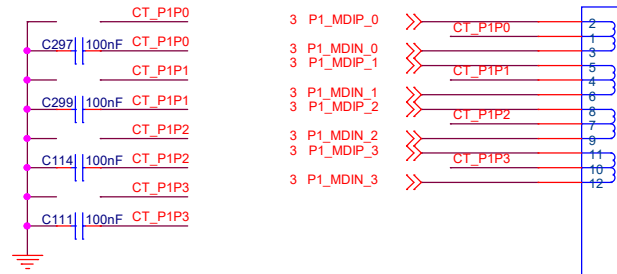
88E6141 Switch

Switch RESET Options:

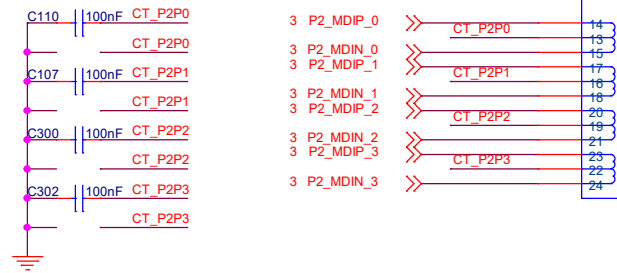


Combo 4 ports 1Gbps connector

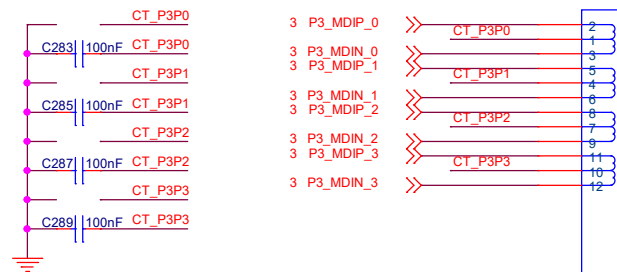
PORT-2 MDI I/F



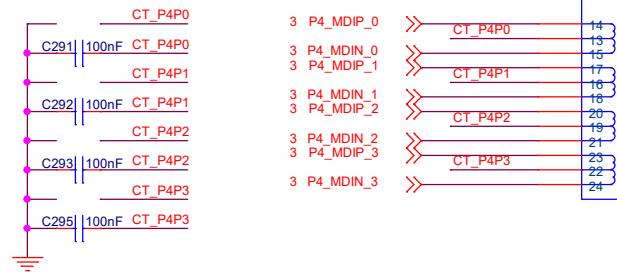
PORT-1 MDI I/F



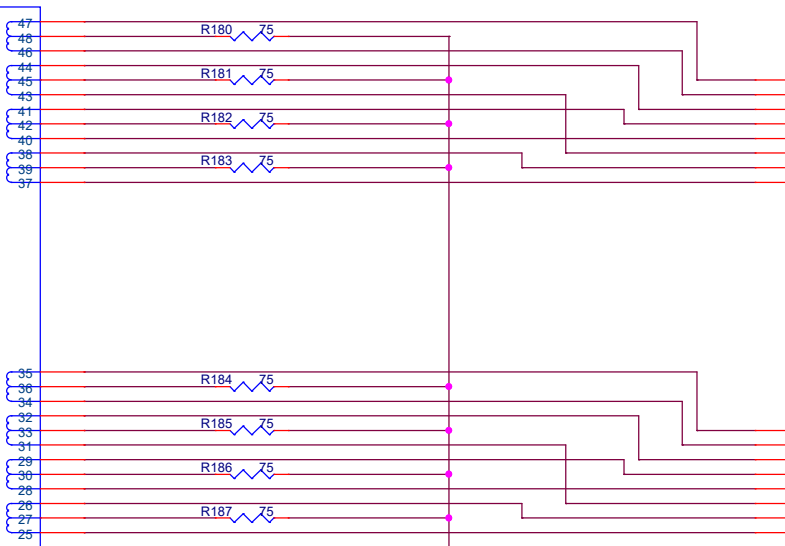
PORT-4 MDI I/F



PORT-3 MDI I/F

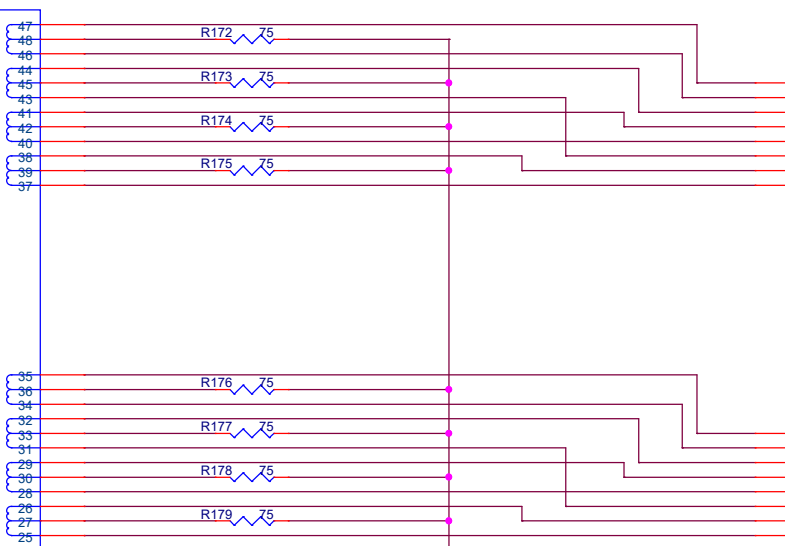


T1
ATPL-453R

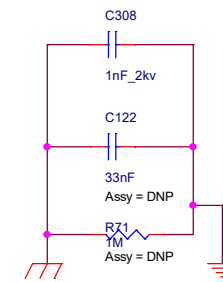
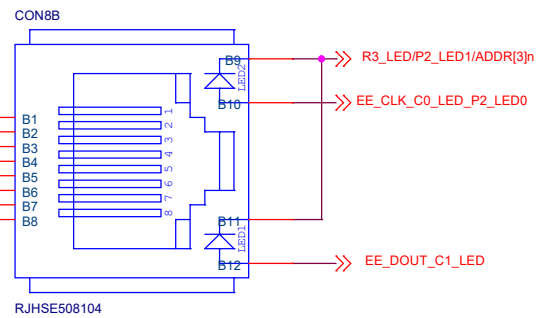
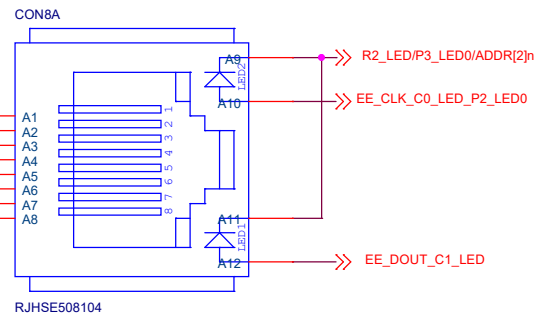
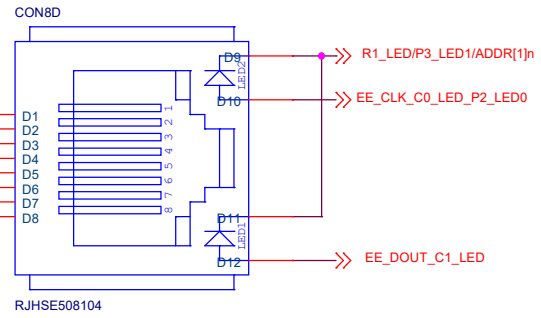
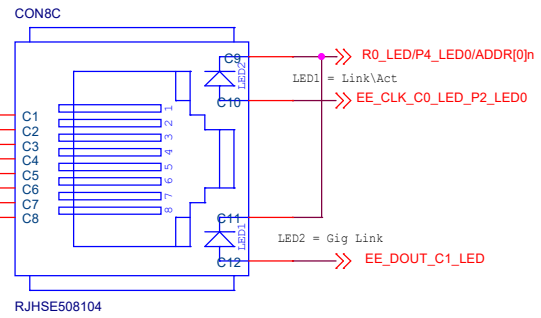


C307
1nF_2kv

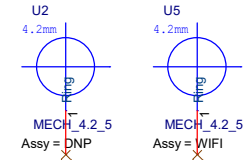
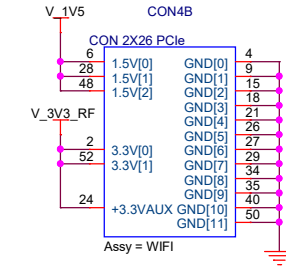
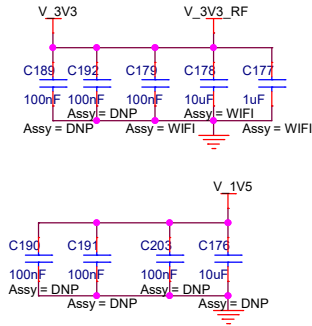
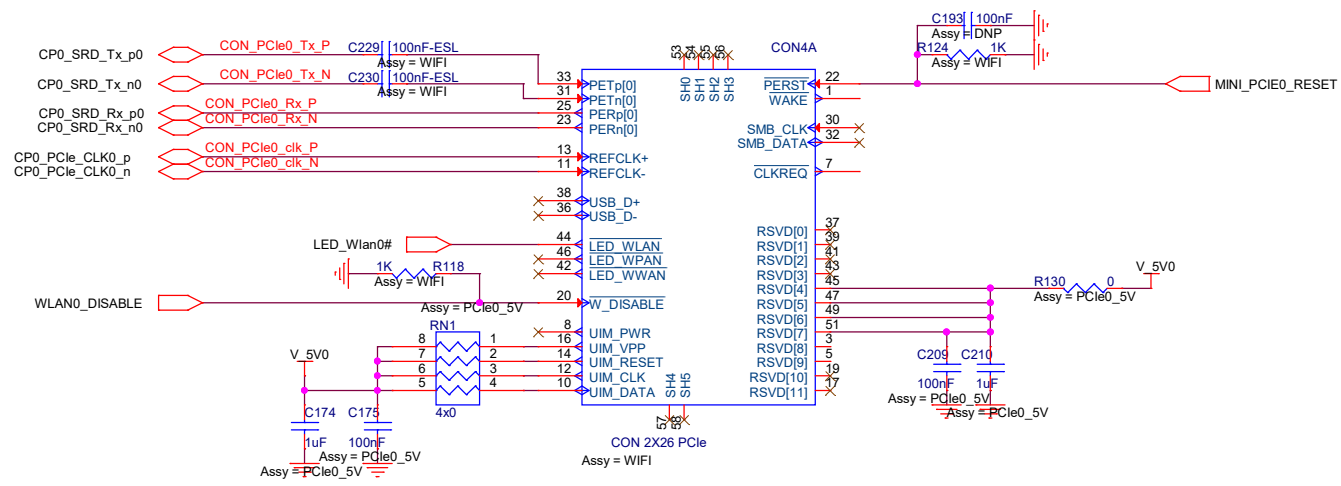
T2
ATPL-453R



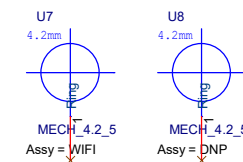
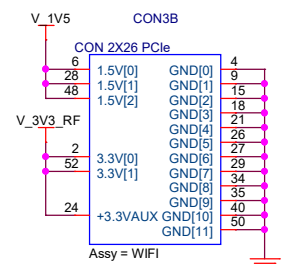
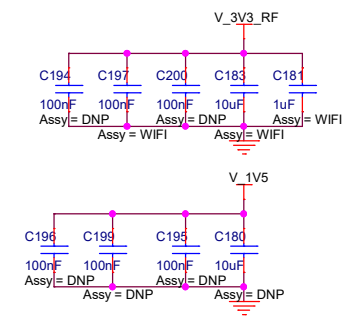
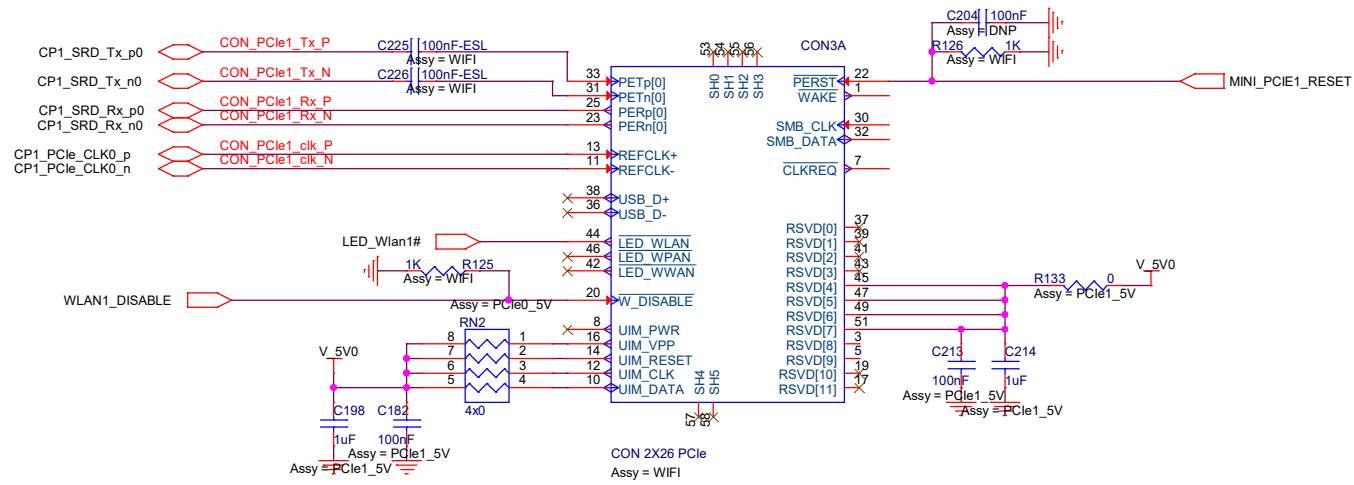
C305
1nF_2kv

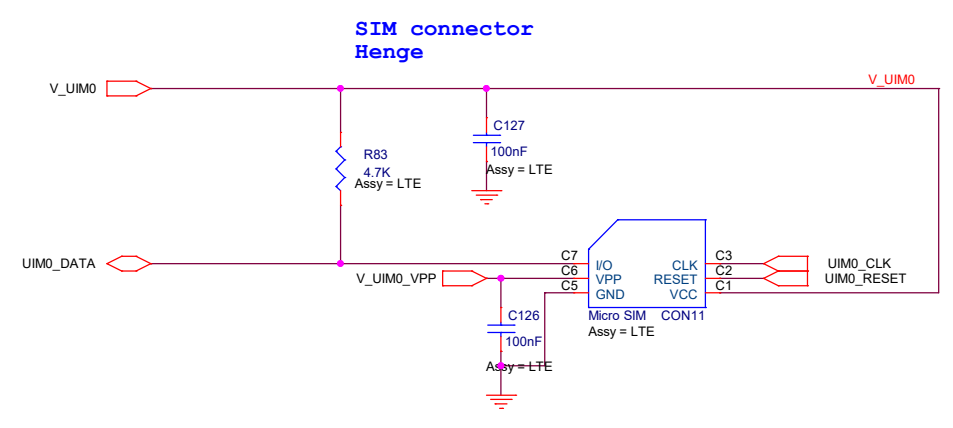
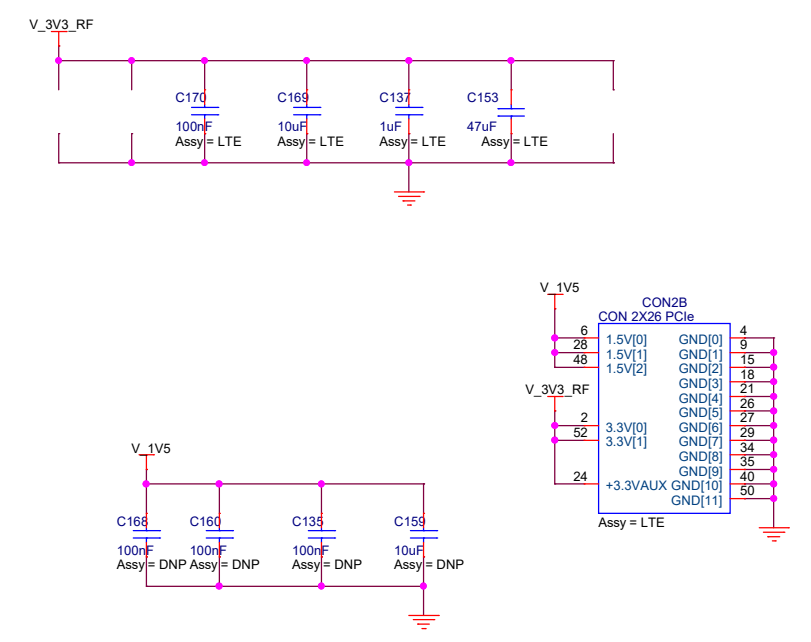
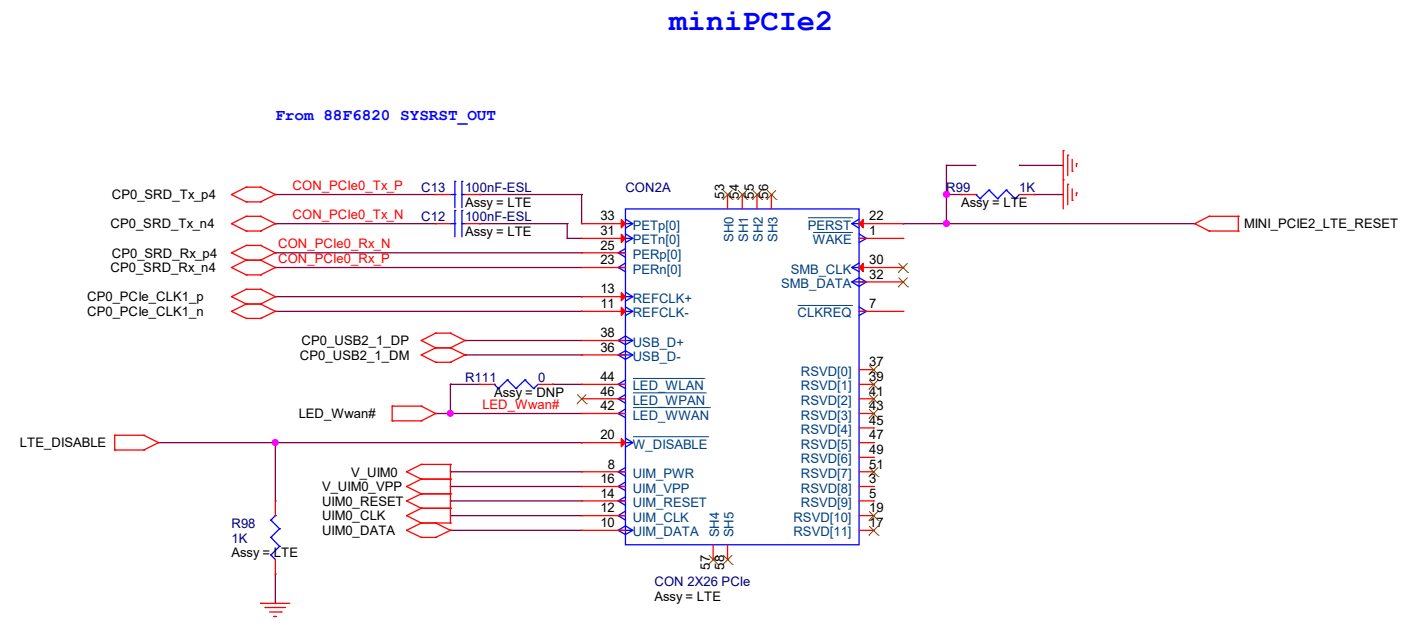


miniPCIe0

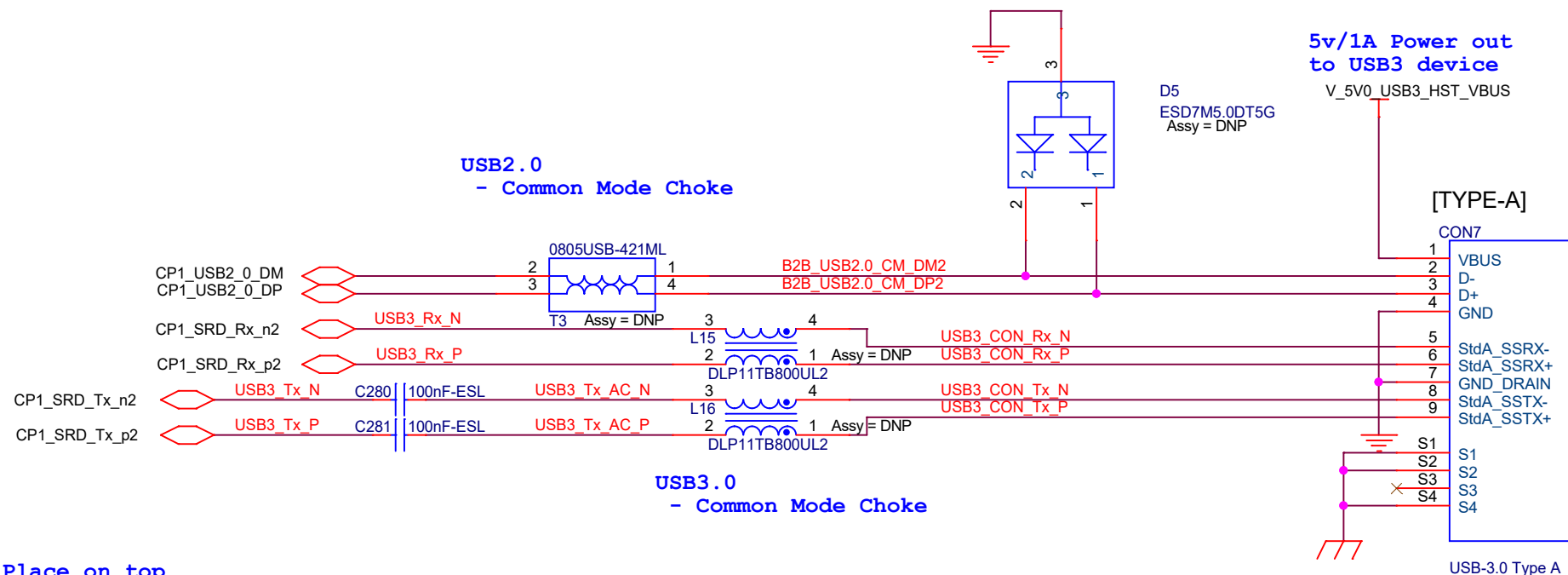


miniPCIe1





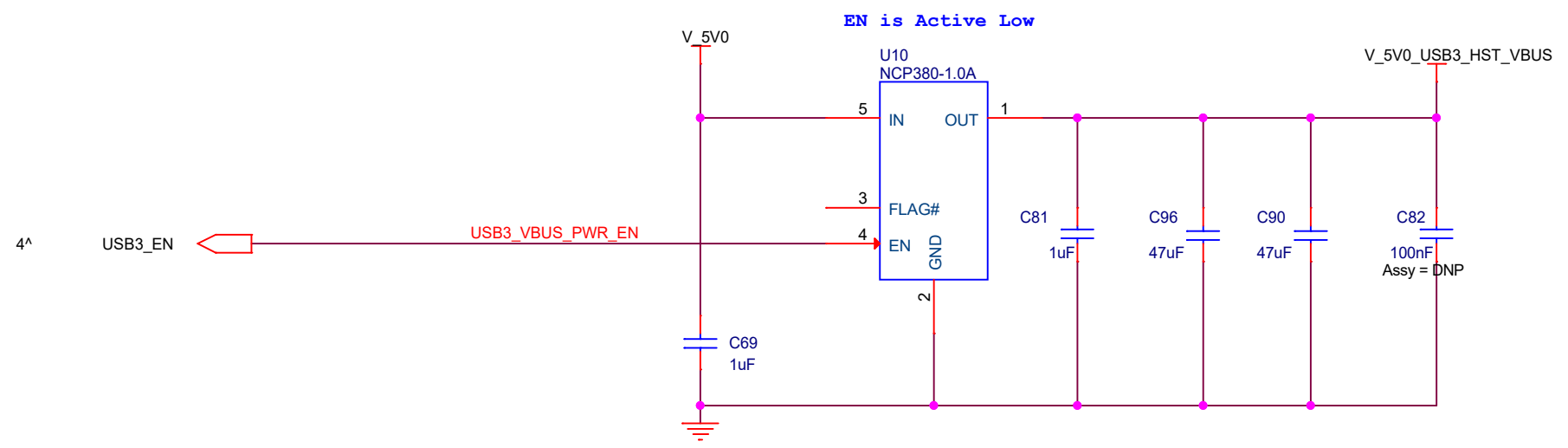
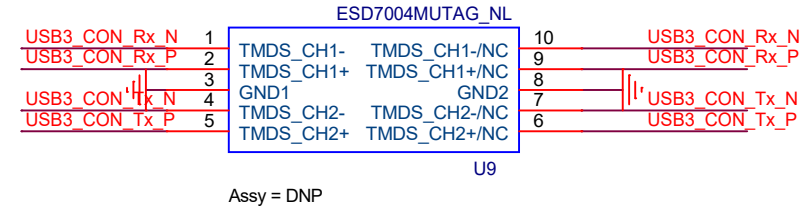
MV USB3.0 HOST



Place on top of common mode choke



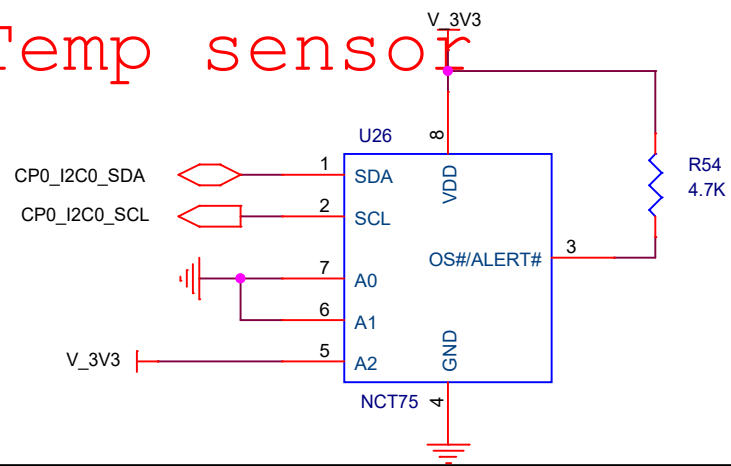
Change connectivity to match layout constraints



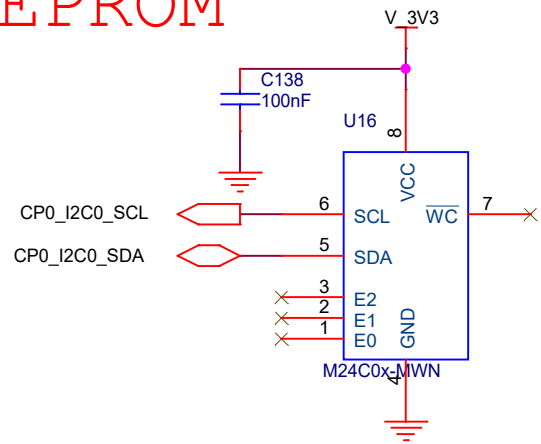
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| | | |
|--------|----------------------------|---------------|
| Size B | Title USB 3.0 connector | Rev 1.1 |
| Date: | Monday, March 11, 2019 | Sheet 9 of 10 |

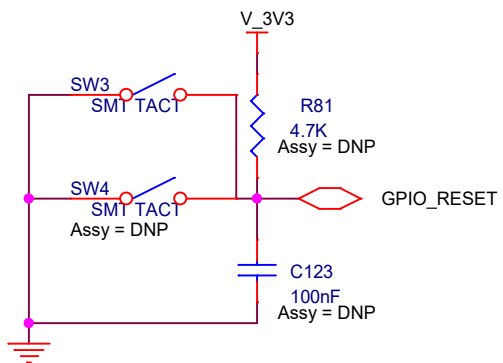
Temp sensor



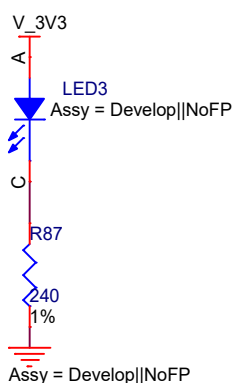
EEPROM



AP reset (GPIO)

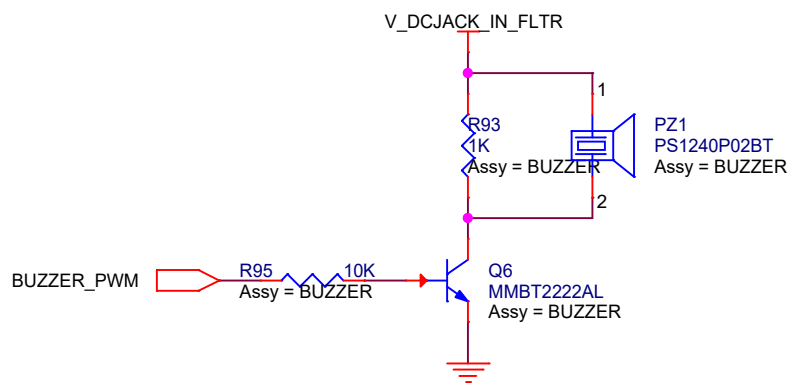


PWR indication

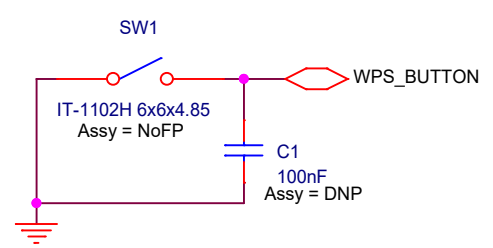


Single tone buzzer

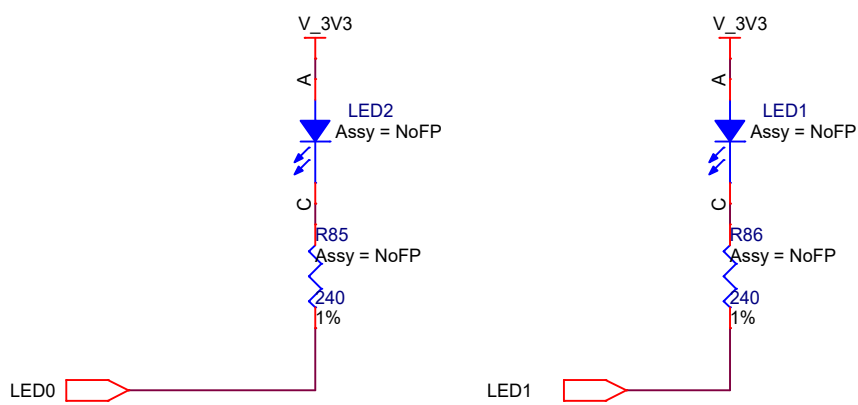
By default not assembled



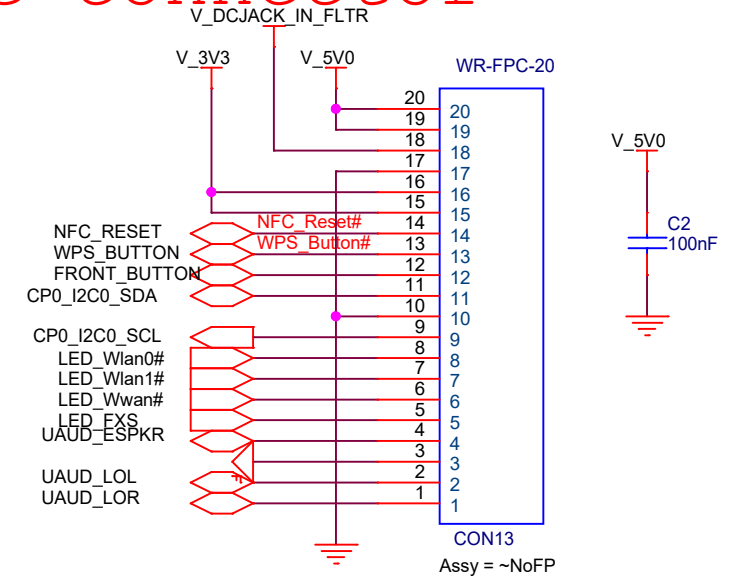
WPS Button (GPIO)



Two GPIO LEDs



Flat cable connector



FAN header (with PWM option)

